DESIGNER'S TOOLKIT

Techniques Simplify Wireless Transmission

Approaches That Were Once Thought Too Costly To Implement Now Have New Life, Thanks To The Availability Of Integrated Devices.

BROADBAND communications equipment is increasingly pushing the envelope of mixed-signal technology in terms of speed, distortion, signal-to-noise ratio (SNR), and cost. Many broadband wireless systems require wideband, low-noise analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with 10 to 14 b of resolution. If architectures aren't carefully considered, these requirements can result in costly solutions.

Digital filtering and processing techniques can reduce the need for expensive analog circuitry. Such techniques include interpolation, decimation, and direct digital synthesis. For example, an architecture that uses multi-rate digital filters and gain stages can be used as part of an image-rejection architecture on both the receive (Rx) and transmit (Tx) paths. With this combination of features, it's possible to reduce component count and lower system cost.

TRANSMIT PATH

The transmit path of a digital transceiver ultimately requires a DAC to create the analog broadcast signal. When a signal is generated by a DAC or undergoes frequency translation using a mixer or upconverter, unwanted duplicate signals are produced. These signals are called images or aliases. Analog low-pass filters can remove these images and other spurious noise from the signal. Practical analog filters can be expensive, however. They also have limitations that require designers to make tradeoffs between transition band size, in-band attenuation, out-ofband attenuation, dimensions, and cost.

Fortunately, digital-processing operations can ease filtering requirements. One technique involves the initial separation of the digital baseband signal into its in-phase and quadrature (I&Q) components. Generally speaking, a great deal can be gained by working with these component signals and converting them to a single analog signal as close to the antenna as possible. Implementing this scheme requires a pair of DACs. The output of these DACs is fed to a quadrature mixer, thereby forming an imagerejecting quadrature upconversion architecture.

Quadrature modulation, which requires precise phase relationships, is not a new concept. More than 40 years ago, it was used to produce single-sideband radio signals. With analog circuitry, however, maintaining quadrature



phase relationships over wide bandwidths is not easily accomplished. These techniques have mostly been used at low IF frequencies, with the aim of removing the redundant sideband and eliminating the "carrier."

The development of low-cost, integrated direct-digital-synthesizer (DDS) circuits has changed the game. Products such as the AD9879, for example, include a DDS that produces digitally precise quadrature output signals (with a typical accuracy of two-tenths of one degree). It operates from dc to greater than 70 MHz using a 210-MHz clock source. That clock source can be derived from a highquality LO if divided-down appropriately. The quadrature phase error of quadrature modulators, like the one in the AD9879, is on the order of one degree over its output range.

An advantage of the DDS system is that its output frequency and phase can be precisely and rapidly manipulated under digital processor control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution. This would include frequency control in the millihertz (mHz) range, as well as phase control of less than 0.09°. The DDS system also has an innate ability to rapidly hop frequencies (up to 23 million output-frequency changes per





2. Using this plot of orthogonal-frequency-divisionmultiplexing (OFDM) signal data, the plots were generated in Figures 3, 4, and 5.



4. This real OFDM signal was obtained through 4x interpolation.



Digital filtering of the baseband signal also can simplify the filtering required later in the signal chain. Generally speaking, increasing the DAC sampling rate can ease anti-alias filter rolloff requirements. While it may be possible to increase the sampling frequency of the DAC simply by using a faster DAC, a more economical alternative is to increase the effective sampling rate of the signal through interpolation.

The interpolation process involves the insertion of zero samples between data samples. The combination of these samples is fed to a finite-impulse-response (FIR) or cascaded-integrators (CIC) digital filter, which can have a low-pass or a bandpass characteristic. The new "zerostuffed" sampling rate is used to update the DAC. This process results in a wider transition band, while easing the requirements of the analog smoothing filter at the output of the DAC. The aliases of the signal appear at a frequency that is higher than the original sampling rate by approximately the interpolation factor.

How do these techniques fit together? One implementation is shown below in FIGURE 1. This block diagram illustrates the transmit path of the AD9860 broadband-modem mixed-signal front end. The AD9860 architecture shows one method of implementing complex mixing. It also copes with the filtering and frequency-tuning issues that are encountered in the superheterodyne upconversion process. As mentioned earlier, quadrature upconversion requires separate I&Q signals. If I&Q signals are not available, they can be created with the use of a phase-shifting Hilbert filter from a low-IF real signal.

This example features a digital two-



3. The DAC output of a real OFDM signal is shown here. It was obtained using various digital-processing features. In this case, that means that it used no digital filtering or mixing.



5. The real OFDM signal shown in this graph was obtained by utilizing a Hilbert filter.

mixer architecture. When used in combination with the first mixer, the DDS provides fine frequency tuning. As mentioned previously, the complex low-IF signal is fed to an interpolation filter to increase the separation between the aliases. The signal is then mixed up to an IF that is the tuned frequency Fs/4 or Fs/8.

Note that a single mixer and DDS combination with a wider tuning range could have been employed in place of the second mixer. This simplified architecture, with a higher-resolution DDS running at a lower rate, is designed for low-cost integration and low power consumption. This approach comes at the expense of more complexity in the interpolation filters. They require a larger pass-band and a smaller transition band.

Figures 3, 4, and 5 show a progression of the effects on the output signal from the various blocks in the signal chain. The same OFDM signal was used to gen-

WIRELESS SYSTEMS DESIGN || JANUARY/FEBRUARY 2003

39

DESIGNER'S TOOLKIT

[DSP DESIGN TECHNIQUES]

erate all of the plots. It is shown in **FIGURE 2**. The OFDM signal data represents a single channel or real signal. It contains 512 carriers with a peak-to-average ratio of 11 dB spanning 6 MHz and centered at 6 MHz. At the center of the signal, 10% of the signal is notched out to provide a figure of merit of performance versus the ideal (70 dB).

FIGURE 3 shows the OFDM signal at the DAC output with no filtering or mixing. It is updating at a rate of 24 MSamples/s. The signal demonstrates a notch depth of about 70 dB (noise floor) or 61 dB (worst spur). The DAC output suffers from SINx/x response that causes an attenuation of about 2 dB over the 6-MHz signal bandwidth. A worst-case image of –6 dBc occurs only 6 MHz away.

In **FIGURE 4**, the output spectrum after a 4x-interpolation filter is applied. The worst image is now attenuated by -20dBc. It is located 78 MHz away from the desired signal. This shifting of the image in combination with the attenuation significantly eases filtering requirements.

In this example, the first step in frequency tuning is done with relatively coarse Fs/4 modulation and the Hilbert filter enabled. The signal is now centered at 30 MHz (Fdac/4 + 6 MHz) with its suppressed negative image at 18 MHz (Fdac/4 - 6 MHz). FIGURE 5 shows the output of the system modulated only with Fs/4. Using a combination of the two mixers and modulators in this architecture, the entire output signal can be placed anywhere up to 73% of Nyquist frequency of the DAC. As previously mentioned, the complex modulator (block B) upconverts the signal to Fdac/4 or Fdac/8. The tunable complex modulator (block D) upconverts in steps of (Fdac/4)/224 using a 24-b tuning word. At an Fdac rate of 96 MHz, the tuning resolution of this system is about 1.43 Hz.

When used as part of a digital communications system, the transmit signal chain illustrated would be connected to a quadrature upconversion mixer, such as the AD8345. The mixer adds the tuned I&Q signals together to complete the image-rejection scheme. At the output of the upconverter, the amount of image and LO suppression realized at IF depends on offset and gain error in the DAC output signals. It also depends on the mismatches of the mixer I&Q paths. Programmable calibration amplifiers can be used to correct for DAC errors and even some of the mixer errors.



6. Shown here is an image-rejection receiver architecture. The transmit path of the AD9860 broadband-modem mixed-signal front end is depicted, along with one method of implementing complex mixing and coping with the filtering and frequency tuning issues.

In a typical superheterodyne receiver, the incoming RF signal is downconverted to a lower frequency before additional processing takes place. In a digital communications system, the signal is digitized using an ADC. The result is a digital signal that can be processed by a DSP or a digital ASIC. An effort is usually made to select an IF that avoids system clocks, their harmonics, and images occurring from the mixing processes.

WHEN BROADBAND WIRELESS SYSTEM ARCHITECTURES AREN'T CAREFULLY CONSIDERED, THE RESULT OF IMPLEMENT-ING AND ADHERING TO SPECIFIC REQUIREMENTS CAN BE VERY COSTLY TO THE OVERALL SYSTEM.

A first IF can be as high as several hundred MHz. Some systems employ a second downconversion to place the signal at a lower IF. The resulting IF will be less than the Nyquist Frequency of the ADC. Each additional mixing stage in superheterodyne receivers requires more mixers, clock synthesizers, filters, and amplifiers. All of this, of course, has a significant impact on the overall system cost. To minimize the number of stages, for example, employ high-sampling-rate ADCs. These ADCs can be used to receive IF-frequency I&Q channels. When combined with digital signal processing, they generate a real signal with image rejection. This implementation could replace a last heterodyne stage implemented with analog circuitry.

A digital technique called decimation can reduce noise and ease the filtering requirements in a digital receiver. A decimation filter allows the ADC to run at a multiple of the original sampling rate. To preserve the data in the original signal, this rate may be much higher than is required. Yet it will output data at the original sampling rate. The higher sample rate decreases the required rolloff rate of anti-alias filters. Decimation filters also attenuate out-of-band signals. They reduce system noise from ADC quantization or other sources as well.

FIGURE 6 shows an image-rejection receiver architecture. In this case, the quadrature downconverter provides analog I&Q signals at its output. These signals are filtered and input to oversampling ADCs. The digital output of the ADCs is then filtered using decimation filters, which reduce the noise and ease the filtering requirements. This step is followed by a Hilbert filter. It re-combines the signals and provides a real digital output signal.

While some of these techniques are not new, they have only recently gained the potential to be realized at low cost. Integrated devices, such as the AD9860 mixed-signal front end (MxFE), allow such complicated techniques to be used in cost-sensitive, high-performance, digital-broadband applications.

Curt Wise, Product Marketing Manager, Analog Devices, Inc., Ray Stata Technology Center, 804 Woburn St., Wilmington, MA 01887; (781) 937-1989, (800) ANALOGD, www.analog.com.

JANUARY/FEBRUARY 2003 || WIRELESS SYSTEMS DESIGN